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# Performance Evaluation of 6 Transistor D-Flip Flop based Shift Registers using GDI Technique

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**Abstract**: Power dissipation is an important parameter in the design of VLSI circuits, and the clock network is responsible for a substantial part of it (up to 50%). Low Power digital CMOS becomes more and more interesting, due to the general advances in process technology and due to new low power applications. As technology advances push for smaller devices and faster operations, power consumption and become severe problems when designing high-speed ICs. These challenging concerns are mainly due to the excessive switching activity in the chip that keeps increasing proportionally to the frequency augment and the number of transistors. In this paper a new 6 transistor D-Flip-Flop based on GDI technique is designed and Shift Registers including Serial in Serial out (SISO), Serial in Parallel out (SIPO), Parallel in Serial Out (PISO), Parallel in Parallel Out (PIPO) are designed based on this newly designed D-Flip-Flop and layouts are also designed using Microwind.

**Keywords**: Flip-Flop, Shift Registers, GDI technique, Power, Layout.

## I. INTRODUCTION

It has been shown that a significant portion (30-60%) of the total power consumption is dissipated in the clock distribution network and flip-flops that constitute ubiquitous elements for digital CMOS ICs design [10]. This power is dissipated in form of heat and radiation which complicate further the design of the circuit. Since the leakage current augments with temperature, the inefficient package cooling technologies used today contribute to drastically boost the power dissipation. The upcoming sections explains about the sequential circuits and the concept of GDI technique

## II. SEQUENTIAL CIRCUITS

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data.

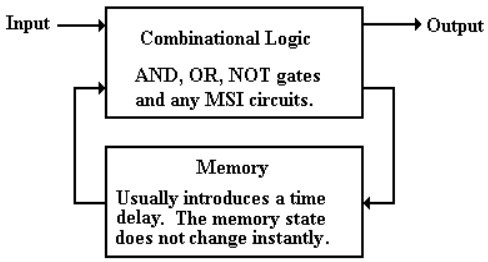


Fig. 1. Representation of Sequential Circuit

Sequential circuits have memory and combinational circuits do not. All sequential circuits contain combinational logic in addition to the memory elements. Sequential circuits are those with memory, also called "feedback". In this, they differ from combinational circuits, which have no memory. The stable output of a sequential circuit depends on the order in which the inputs are changed. Sequential circuits can be used as memory elements; binary values can be stored in them.

### *A. MUX based D-Flip-Flop*

The flip-flop used in this paper is the double edge triggered flip-flop. The principle incorporated in the flip flop is that during the rising edge of the clock, the input value gets delayed with reference to the clock signal fed.

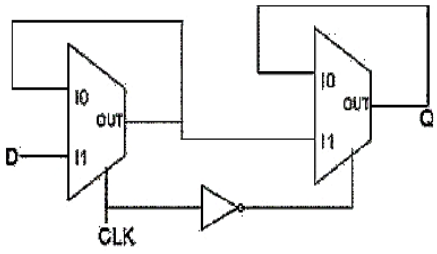


Fig. 2. MUX Based D-Flip-Flop

### *B. Serial in Serial out Shift Register*

The serial in/serial out shift register accepts data serially that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

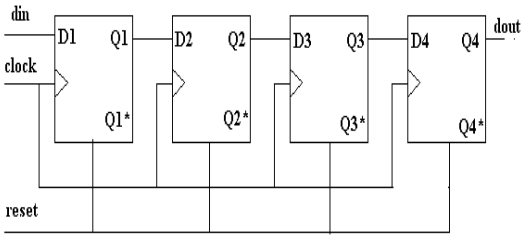


Fig. 3. Serial in Serial out Shift Register

### *C. Serial in Parallel out Shift Register*

This configuration allows conversion from serial to parallel format. Data is input serially, as described in the

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SISO section above. Once the data has been input, it may be either read off at each output simultaneously, or it can be shifted out and replaced. Serial in parallel out diagram is shown in fig.4 For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register.

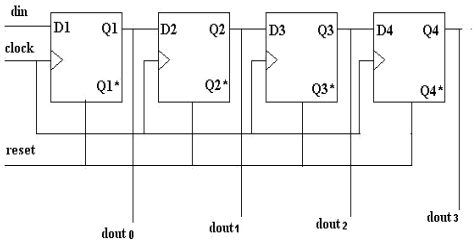


Fig. 4. Serial in Parallel out Shift Register

*D. Parallel in Parallel out Shift Register*

For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by d flip-flops and shown in fig 5. Both the inputs as well as the outputs performs the parallel operation. A global clock is given to activate all the flip flops connected as shown below. The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the d inputs appear at the corresponding q outputs simultaneously.

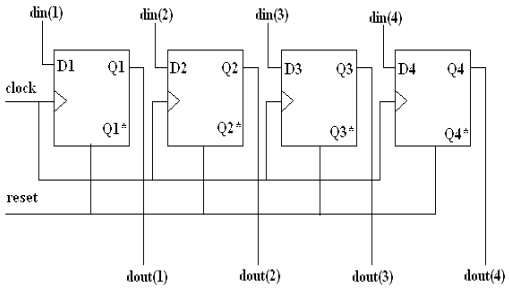


Fig. 5. Parallel in Parallel out Shift Register

*D. Parallel in Serial out Shift Register*

This configuration has the data input on lines d1 through d4 in parallel format. To write the data to the register, the write/shift control line must be held low. To shift the data, the w/s control line is brought high and the registers are clocked. The arrangement now acts as a PISO shift register, with d1 as the data input. However, as long as the number of clock cycles is not more than the length of the data-string, the data output, q, will be the parallel data read off in order as shown in Fig.6.

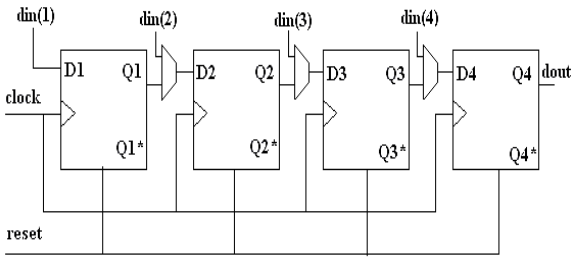


Fig. 6. Parallel in Serial out Shift Register

## III. GROUND DIFFUSION INPUT TECHNIQUE

The GDI technique is of more important because it uses only couple of transistors to construct a design. As the operation involves only two transistors, it could show better results in terms of Power Dissipation, Speed as well as the area occupied. This technique is most predominant for designing circuits in MOSFET technology. A basic GDI cell contains four terminals – G node (the common gate input of the nMOS (Negative channel Metal-Oxide Semiconductor) and pMOS (Positive channel Metal-Oxide Semiconductor) transistors), P node (the outer diffusion node of the pMOS transistor), N node (the outer diffusion node of the nMOS transistor), D node (the common diffusion of both transistors). P, N and D may be used as either input or output nodes, depending on the circuit structure shown in Fig.7. Multiple-input gates can be implemented by combining several GDI cells .GDI enables simpler gates, lower transistor count, and lower power consumption in many implementations. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The overall area and complexity of the circuit is minimized using GDI technique. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors per function) in GDI design method.

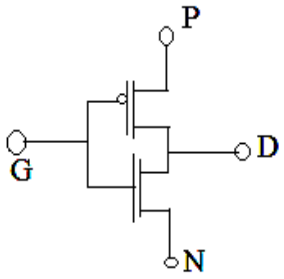


Fig. 7. Symbol of GDI Cell

## IV. PROPOSED D-FLIP-FLOP AND SHIFT REGISTERS USING GDI TECHNIQUE

*A. Proposed 6 transistor D-Flip-Flop*

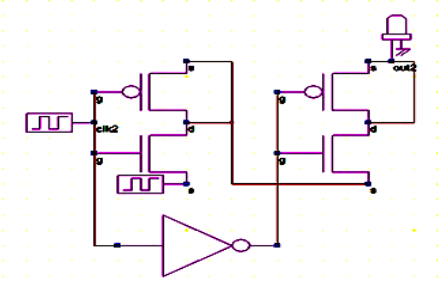

Fig. 8. Proposed 6 transistor D-Flip-Flop

*B. Proposed Serial in Serial out Shift Register*

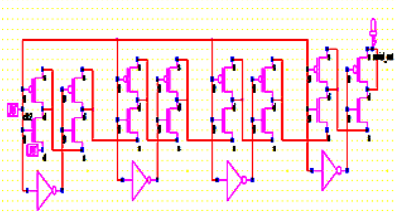

Fig. 9. Proposed Serial in Serial out Shift Register

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*C. Proposed Serial in Parallel out Shift Register*

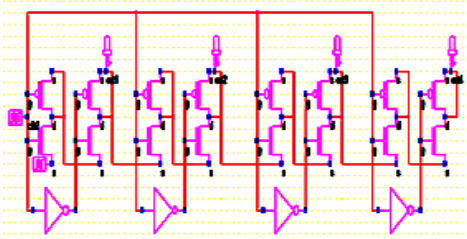

Fig 10. Proposed Serial in Parallel out Shift Register

*D. Proposed Parallel in Serial out Shift Register*

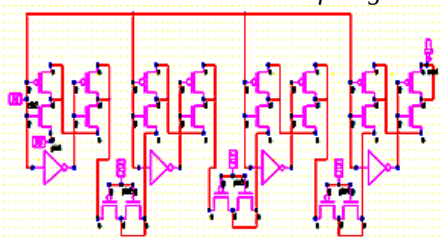

Fig. 11. Proposed Parallel in Serial out Shift Register

*E. Proposed Parallel in Parallel out Shift Register*

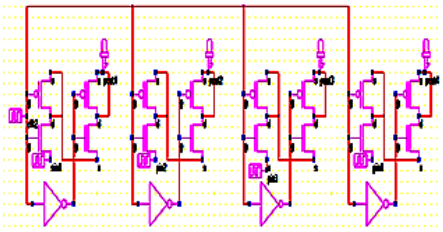

Fig. 11. Proposed Parallel in Parallel out Shift Register

## V. SIMULATION OUTPUT WAVEFORMS

*A. Proposed 6 transistor D-Flip-Flop*

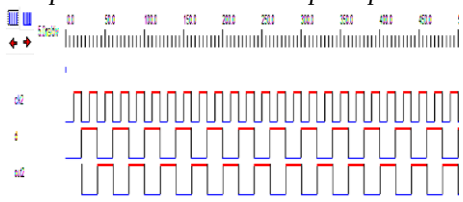

Fig. 13. Simulation output of proposed Flip-Flop

*B. Proposed Serial in Serial out Shift Register*

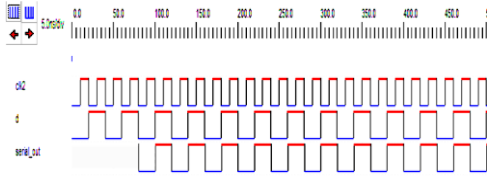

Fig. 14. Simulation output of proposed SISO

*C. Proposed Serial In Parallel Out Shift Register*

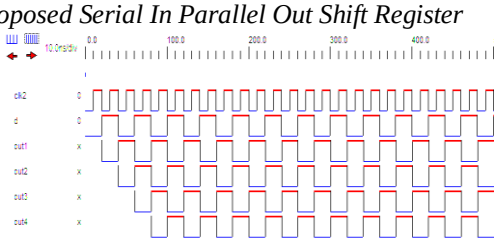

Fig. 15. Simulation output of proposed SIPO

*D. Proposed Parallel in Serial Out Shift Register*

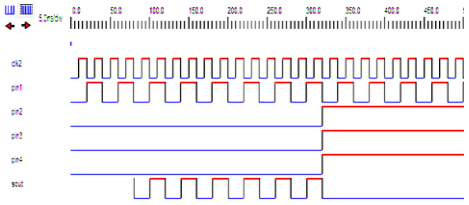

Fig. 16. Simulation output of proposed PISO

*E. Proposed Parallel In Parallel Out Shift Register*

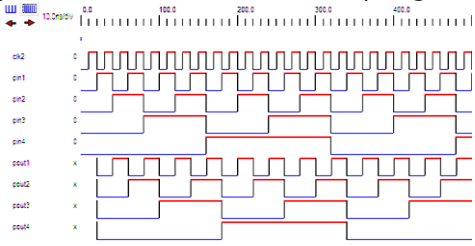

Fig. 17. Simulation output of proposed PIPO

## VI. LAYOUT OF FLIP-FLIP-FLOP AND SHIFT REGISTER

*A. Proposed D-Flip-Flop*

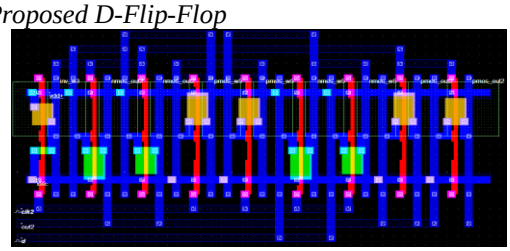

Fig. 18. Layout of proposed D-Flip-Flop

*B. Proposed Serial in Serial out Shift Register*

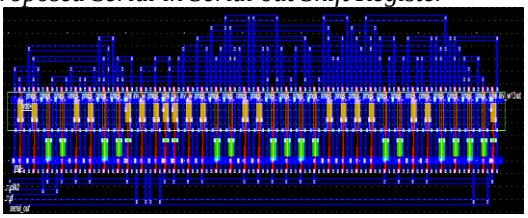

Fig. 19. Layout of proposed SISO

*C. Proposed Serial in Serial out Shift Register*

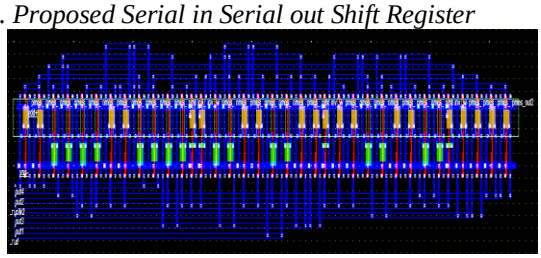

Fig. 20. Layout of proposed SIPO

*D. Proposed Parallel in Parallel out Shift Register*

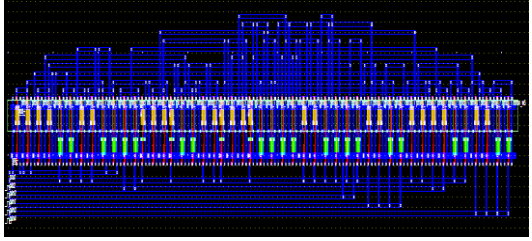

Fig. 21. Layout of proposed PISO

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### F. *Proposed Parallel in Parallel out Shift Register*

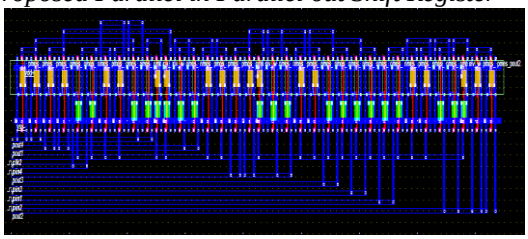

Fig. 22. Layout of proposed PIPO

TABLE I. POWER ANALYSIS

| Design | Power (mW) |
|---|---|
| D-Flip-Flop | 0.002 |
| Serial In Serial Out Shift Register | 0.021 |
| Serial In Parallel Out Shift Register | 0.021 |
| Parallel In Serial Out Shift Register | 0.021 |
| Parallel In Parallel Out Shift Register | 0.020 |

## VII. CONCLUSION

Thus the D-Flip-Flop with 6 Transistors using the GDI technique is designed and shift Registers are also designed with the above descripted 6 Transistor D-Flip-Flop. It predominantly consumes very less Power compared with the conventional Flip Flop designs. The transistor count is also minimized and results in occupying of very low area. The design can also perform faster. The high end digital circuits designed with these Flip-Flop and Shift Registers will definitely show better results compared to normal designs.

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**Mathan.N** was born in Nagercoil, Tamilnadu, India in 1989. He received his Bachelor Degree in Electronics and Communication Engineering from Anna University, Chennai in the year 2010. Master Degree in VLSI Design from Sathyabama University, Chennai in the year 2013. He is working as Assistant Professor in Department of ECE in Sathyabama University. His interested areas are Nano Electronics, VLSI Design, Low Power VLSI Design, Testing of VLSI circuits and Advanced Digital System Design. He has Research publications in National / International Journals /Conferences.